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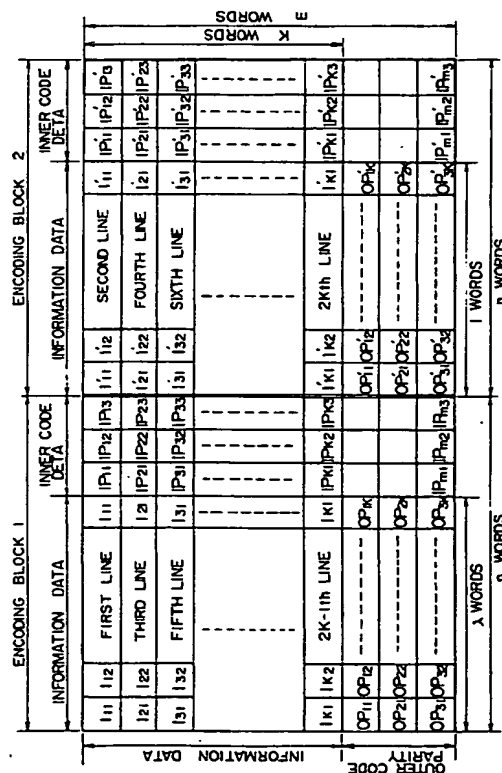
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London WC1R 5DJ (GB)(54) **Error correction code encoder and decoder.**

(57) A product code is generated by first encoding means for generating a first error correction code which is a first parity code added to a first code group having a predetermined number of consecutive information codes of a code sequence, and second encoding means for generating a second error correction code which is a second parity code added to a second code group having information codes each derived from a first group among a plurality of consecutive code groups of the code sequence. An error correction code having a high burst error correction capability can thus be realized without using an additional interleave circuit and other circuits.

FIG. 5

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to an error correction code encoder and decoder, and more particularly to an encoder and decoder using a so-called product code as an error correction code in a system which transmits a code train via a transmission path such as a magnetic recording/reproducing path which may sometimes generate burst errors.

Related Background Art

It is known that a so-called interleave method is used to improve an error correction capability of a system having a transmission path such as a magnetic recording/reproducing path which may sometimes generate burst errors. With this interleave method, data after being subject to error correction code encoding and constituting the same encoded block or same error correction code, is distributedly sent to a transmission line.

Such an interleave method used by a video VTR will be described by way of example.

Fig. 1 is a diagram used for explaining a video signal processed by a digital VTR. In Fig. 1, there are shown horizontal scan lines including the first, second, ..., 525-th line. In this example, a video signal having 525 horizontal scan lines such as an NTSC signal is used.

In VTR, digital video signals of one frame are divided into a predetermined number (P) of blocks. Each block is subject to error correction code encoding, and written in one track. Namely, P tracks are used for recording video signals of one frame.

Fig. 2 is a diagram illustrating error correction code encoded blocks. As shown in Fig. 2, information data (information words) I_{11} to I_{ki} is encoded by using such as Reed Solomon codes to provide inner codes in the horizontal direction and outer codes in the vertical direction, i.e., provide so-called product codes. In this example, it is assumed that inner and outer codes include three parity words (check bits) IP_{11} to IP_{3m} and OP_{11} to OP_{3k} , respectively, and that each code can correct one word error.

The order of recording data (order of data transmission) in a magnetic tape is the same as the direction of inner code encoding, i.e., in the order of I_{11} , I_{12} , I_{13} , ..., I_{1i} , IP_{11} , IP_{12} , IP_{13} , I_{21} , I_{22} , Therefore, burst errors caused by dropout by scratches or stains of a magnetic tape during a reproducing operation are consecutive in the inner code encoding direction.

As described above, if each outer or inner code can correct one word, burst errors of maximum one line or i words can be corrected by outer codes, but burst errors more than this cannot be corrected.

In order to improve the error correction capability,

data is encoded for each block. The encoded data is exchanged between blocks to record mixed data of a plurality of blocks in one track. For example, in a simple case, data of two blocks is exchanged on the line unit basis. With such an arrangement, even if burst errors more than one line occur, burst errors of maximum two lines can be corrected using outer codes because the reproducing process can be performed one line per each block. However, in this case, two tracks for the unit interleave process should not contain other burst errors or random errors. It can be said therefore that the above-described interleave method is very effective for improving the error correction capability without having a large redundancy if occurrence frequency of burst errors is low to a certain degree.

Fig. 3 is a block diagram showing the brief arrangement of a conventional digital VTR which uses the interleave method.

Information data inputted from an input terminal 300 is encoded on the block unit basis by an outer code encoding circuit 301 and inner code encoding circuit 302. The data is exchanged or interleaved in line unit or word unit at an interleave circuit 303 by using a memory. The interleave circuit 303 sequentially outputs data of a plurality of blocks to a recording circuit 304 which processes the data for magnetically recording it in a magnetic tape (recording medium) 310 serving as a transmission path.

A signal picked up from the magnetic tape 310 is supplied to a reproducing circuit 305 to reproduce data. The reproduced data is processed by a de-interleave circuit 306 in the manner opposite to the interleave circuit 303, and sequentially outputted one line after another in units of block such as shown in Fig. 2. The outputted data is subject to error correction processes at an inner code decoding circuit 307 and outer code decoding circuit 308 using inner and outer codes. The error-corrected digital video signal is outputted from an output terminal 309.

The above-described digital VTR requires address generators, memories, and the like, which are used for the interleave process only, resulting in an increase of hardware.

Furthermore, the order of data before encoding is different from the order of data on a magnetic tape (on a transmission line). Therefore, a desired data order before error correction code encoding cannot be recorded (transmitted) as it is. In a special reproducing mode of a digital VTR, such as a high speed search which reproduces data while transporting a tape at a speed different from that when recording it, a particular data order is used for, allowing effective pixel reproduction. This particular data order of video signals changes if error correction code encoding is performed. It becomes therefore necessary to rearrange the data after error correction code encoding, or to determine a data order while considering

such change in advance. In the former case, complicated processing is required, and moreover this processing is carried out with parity bits (words) being affixed so that data amount to be processed becomes bulky and the amount of hardware increases. Also in the latter case, complicated processing is required, a time required for data exchange may become longer, and the amount of hardware increases.

SUMMARY OF THE INVENTION

In consideration of such circumstances, it is an object of the present invention to provide an error correction code encoder and decoder having a high error correction capability without increasing hardware so much.

In order to achieve the above object of the present invention, there is presented an embodiment of an error correction code encoding device, comprising:

(a) first encoding means for generating a first error correction code which is a first parity code added to a first code group having a predetermined number of consecutive information codes of a code sequence; and

(b) second encoding means for generating a second error correction code which is a second parity code added to a second code group having information codes each derived from a first group among a plurality of consecutive code groups of the code sequence.

There is also presented an embodiment of an error correction code decoding device, comprising:

(a) first decoding means for decoding a first error correction code which is a first parity code added to a first code group having a predetermined number of consecutive information codes of a code sequence; and

(b) second decoding means for decoding a second error correction code which is a second parity code added to a second code group having information codes each derived from a first group among a plurality of consecutive code groups of the code sequence.

The other objects and advantages of the present invention will become more apparent from the following detailed description of the embodiments when read in connection with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a diagram used for explaining a video signal used in a digital VTR;

Fig. 2 is a diagram showing error correction code encoded blocks of a conventional digital VTR;

Fig. 3 is a block diagram showing the brief arrangement of a conventional digital VTR;

Fig. 4 is a schematic diagram showing the main part of a recording system of a VTR according to

an embodiment of the present invention;

Fig. 5 is a diagram showing the structure of error correction code encoded blocks used for explaining an error correction code encoding method used by VTR shown in Fig. 4;

Fig. 6 is a diagram showing a recording state of a tape used by VTR shown in Fig. 4; and

Fig. 7 is a schematic diagram showing the main part of a reproducing system for VTR shown in Fig. 4.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

An embodiment of the present invention applied to a digital VTR will be described.

Fig. 4 is a schematic diagram briefly showing the main part of a recording system of a digital VTR according to an embodiment of the present invention.

In Fig. 4, reference numeral 100 represents an input terminal for a digital video signal. Like an ordinary television signal, data of each frame, each field, and each line is time sequentially inputted. Reference numeral 101 represents a special reproduction interleave circuit which changes a time sequential inputted digital video signal into a form suitable for a special reproduction such as high speed search. The structure of such a special reproduction interleave circuit can be realized using the teachings given in Japanese Patent Publication No. 63-55541 and U.S. Serial No. 317,430 filed on March 1, 1989. The structure of the circuit is not directly related to the present invention, so the detailed description thereof is omitted. It is assumed in this embodiment that the interleave circuit 101 interleaves data on the line unit basis.

Reference numeral 140 represents an outer code encoding circuit which receives a data train from the special reproduction interleave circuit 101. The data train with outer code parities added by the outer code encoding circuit 140 is inputted to an inner code encoding circuit 150 which further adds inner code parities.

Fig. 5 is a diagram showing encoded blocks used for explaining the error correction code encoding method used by VTR of this embodiment. Data on the first to 2k-th lines are sequentially inputted to the outer code encoding circuit 140 in this order. As shown in Fig. 5, it is assumed that three parity words are added as outer codes and as inner codes, respectively, and that each parity word can correct one word at the maximum.

Referring to Fig. 4, the data from the special reproduction interleave circuit 101 is inputted in parallel to a delay circuit 102, P0 parity calculation circuit 110, P1 parity calculation circuit 120, and P2 parity calculation circuit 130.

The structures of the parity calculation circuits 110, 120, and 130 are the same except that coeffi-

icients of generation matrix coefficient tables 112 are different. The three parity calculation circuits calculate three parity words.

The operation of the parity calculation circuit will be described using the P0 parity calculation circuit 110 as an example. The information data supplied to the circuit 110 is inputted to a multiplier 111 on a Galois field. The generation matrix coefficient table 112 is constructed of a ROM and an address controller to sequentially output a coefficient of the generation matrix. The multiplier 111 multiplies the information data (word) by a coefficient outputted from the table 112, on a Galois field. An output of the multiplier 111 is supplied to an adder 113 constructed of an exclusive OR gate, and added to an addition result before two lines supplied from a two-line delay circuit 114. The adder 113 and two-line delay circuit 114 constitute an accumulator which accumulates the multiplication results between information words and coefficients at every second lines.

The above-described processes are executed for all information words I_{11} to I_{ki} and I'_{11} to I'_{ki} i.e., information words for $2k$ lines. Thus, outer codes different between odd lines and even lines are generated as shown in Fig. 5. outer code parity words P0 (OP_{11} to OP_{1k} shown in Fig. 5) are generated for odd line information codes, and outer code parity words P0 (OP'_{11} to OP'_{1k} shown in Fig. 5) are generated for even line information codes. The generated parity words are stored in the delay circuit 114. Reference numeral 115 represents a buffer.

Similarly, the two-line delay circuits of the P1 and P2 parity calculation circuits 120 and 130 store therein outer code parity words P1 and P2 (OP_{21} to OP_{2k} , OP_{31} to OP_{3k} in Fig. 5) for odd line information codes and outer code parity words P1 and P2 (OP'_{21} to OP'_{2k} , OP'_{31} to OP'_{3k} in Fig. 5) for even line information codes.

The delay circuit 102 provides the information data with a delay time corresponding to the time required for processing one word by the parity calculation circuit 110, 120, 130, and outputs the information data for the first to $2k$ -th lines in the order of having been inputted. The portion where inner code parity words are inserted is made undefined.

After the information data ($2k \times i$ words) of the two sets of blocks shown in Fig. 5 has been outputted, the parity words stored in the two-line delay circuits of the parity calculation circuits 110, 120, and 130 are sequentially outputted via the buffers in the order of P0, P1, and P2 so that outer code parity words for six lines are outputted and added to respective $2k$ -lines information codes.

An output of the outer code encoding circuit 140 is supplied to an inner code encoding circuit 150 and added with inner code parity words for each line, the inner code parity words being calculated in the well known manner. The information words for $2k$ lines, $6k$

outer code parity words, and $6m$ inner code parity words are supplied to a recording circuit 160 sequentially for each line of the two sets of blocks shown in Fig. 5. These words are distributedly written on two tracks of a magnetic tape as shown in Fig. 6.

With the error correction code encoding described above, even if burst errors of maximum two lines are present, each one word error can be corrected by using a corresponding one of outer codes. This improvement on error correction capability is the same as the conventional case wherein the dedicated interleave circuit 303 is additionally provided. The order of information codes is not-changed at all throughout the circuit path from the input stage of the outer code encoding circuit 140 to the input stage of the recording circuit 160, without influencing the order of information codes (video data) given by the specific reproduction interleave circuit 101. Thus, it is not necessary to rearrange the order of k information codes after the error correction code encoding, making small the hardware amount of the specific reproduction interleave circuit 101. Various interleave rules can be considered for the specific reproduction interleave circuit 101. In general, data is distributed in units of line to a plurality of tracks constituting one frame, and the data of one frame is thinned in units of line and uniformly distributed to each track.

Fig. 7 briefly shows an example of the arrangement of the main part of a reproducing recording system for code trains encoded as described above. Reference numeral 200 represents a reproducing circuit which reproduces code trains recorded on a magnetic tape shown in Fig. 6.

The reproduced code train is supplied to an inner code decoding circuit 250 which calculates a syndrome of one line information words and three parity words so that an error is corrected by inner codes. Then, the code trains, i.e., information words with errors corrected by inner codes and outer code parity words, are supplied in parallel to a delay circuit 201, S0 syndrome calculation circuit 210, S1 syndrome calculation circuit 220, and S2 syndrome calculation circuit 230, one line after another.

The structures of the syndrome calculation circuits 210, 220, and 230 are the same except that coefficients of check matrix coefficient tables 212 are different. The three syndrome calculation circuits calculate three syndromes S0, S1, and S2.

The operation of the syndrome calculation circuit will be described using the S0 syndrome calculation circuit 210 as an example.

The information data supplied to the syndrome calculation circuit 210 is inputted to a multiplier 111 on a Galois field. The check matrix coefficient table 212 is constructed of a ROM and an address controller to sequentially output a coefficient of the check matrix. The multiplier 211 multiplies the inputted word by a coefficient outputted from the table 212, on a Galois

field. An output of the multiplier 211 is supplied to an adder 213 constructed of an exclusive OR gate, and added to an addition result before two lines supplied from a two-line delay circuit 214. The adder 213 and two-line delay circuit 214 constitute an accumulator which accumulates the multiplication results between information words, parity words and coefficients at every second lines.

The above-described processes are executed for all information words I_{11} to I_{ki} and I'_{11} to I'_{ki} and parity words OP_{11} to OP'_{3k} , OP_{11} to OP'_{3k} , for two lines. Thus, different syndromes S_0 are calculated for odd lines and even lines.

The above-described processes are carried out by the syndrome calculation circuits 210, 220, and 230, so that syndromes S_0 , S_1 , and S_2 for all outer codes are calculated, which are stored in two-line delay circuits within the circuits 210, 220, and 230.

An error correction circuit 203 corrects errors of the information data supplied from the delay circuit 201 via a buffer 202, by using syndromes S_0 , S_1 , and S_2 supplied from the syndrome calculation circuits 210, 220, and 230 via buffers 215, in the well known manner. If each outer code can correct one word, consecutive errors within two lines ($2n$ words) generated by the reproducing circuit 200 can be corrected by the outer code decoding circuit 240.

The first to $2k$ -th line information words are outputted from the outer code decoding circuit 240 in the order of having been reproduced, in the manner same as conventional. The order of the outputted information words is rearranged to recover the original order by a specific reproduction de-interleave circuit 204 which executes an rearrangement opposite to that of the specific reproduction interleave circuit 101, and outputted from an output terminal 205.

A VTR having an encoder and decoder described above can improve the burst error correction capability of outer codes by using a different capacity of delay circuit's within the encoder and decoder. Error correction is performed within the processes of the encoder and decoder using error correction codes including outer and inner codes. Therefore, the hardware amounts of both the recording system (encoding system) and reproducing system (decoding system) will not become large while dispensing with a dedicated interleave circuit. Furthermore, such processes will not change the order of information code trains, without influencing a specific reproduction interleave.

In the above embodiment, inner codes are disposed in the direction same as the direction of occurrence of burst errors. Namely, inner codes are added to consecutive information codes of i words (one line), and outer codes are obtained basing upon words derived at every second lines in the direction different from the first-mentioned direction. Instead, outer codes may be obtained basing upon words at each

line, and inner codes may be obtained basing upon words derived at every second lines, with the similar advantageous effects being ensured. In other words, first and second error correction codes may be inner and outer codes, or vice versa.

In the above embodiment, outer codes (second error correction codes) are obtained basing upon information words derived at every second lines, i.e., information words derived in the vertical direction of the data matrix shown in Fig. 5. Outer codes may be obtained basing upon information words derived in the oblique direction of the matrix, i.e., second codes (outer codes) may be obtained basing upon information words each derived from $2i$ consecutively transmitted information words, with the similar advantageous effects being ensured.

Furthermore, in the above embodiment, as shown in Fig. 6, $3k$ outer code parity words are written concentrated on a magnetic tape at every second tracks. It is possible to distributedly allocate outer code parity words by increasing the capacity of the delay circuits 102 and 201 shown in Figs. 4 and 7. In this case, in addition to the above-described advantageous effects, errors at the reproducing circuit 200 can be reduced by decreasing the d.c. components of a code train.

As described so far, according to the present invention, it is possible to realize an error correction code encoder and decoder having a high burst error correction capability without increasing the hardware amount to much extent.

Claims

1. An error correction code encoding device, comprising:
 - (a) first encoding means for generating a first error correction code which is a first parity code added to a first code group having a predetermined number of consecutive information codes of a code sequence; and
 - (b) second encoding means for generating a second error correction code which is a second parity code added to a second code group having information codes each derived from a first group among a plurality of consecutive code groups of said code sequence.
2. A device according to claim 1, further comprising transmission means for transmitting said code sequence added with said first and second parity codes to a transmission path, without changing the order of information codes of said code sequence.
3. A device according to claim 1, wherein said information code is video information, and the infor-

mation amount of said first code group corresponds to said video information of one horizontal scan line.

4. A device according to claim 1, wherein said first error correction code is an inner code, and said second error correction code is an outer code.
5. An error correction code encoding device, comprising:
 - (a) first encoding means for generating a first error correction code which is a first parity word added to a first word group having i consecutive information words of a code sequence, where i is an integer 2 or larger; and
 - (b) second encoding means for generating a second error correction code which is a second parity word added to a second word group having k information words each derived from $(j \times i)$ consecutive information word trains of said code sequence, where j and k are integers greater or equal to 2.
6. A device according to claim 5, wherein said second encoding means includes a multiplier for multiplication of said information word by a generation matrix, and an accumulator including a delay circuit having a delay time longer than a period corresponding to $(j - 1) \times i$ words and an adder.
7. An error correction code decoding device, comprising:
 - (a) first decoding means for decoding a first error correction code which is a first parity code added to a first word group having i consecutive information words of a code sequence, where i is an integer greater or equal to 2; and
 - (b) second decoding means for decoding a second error correction code which is a second parity code added to a second word group having k information words each derived from $(j \times i)$ consecutive information word trains of said code sequence, where j and k are integers greater or equal to 2.
8. A device according to claim 7, further comprising reception means for receiving said code sequence having said information words added with said first and second parity words from a transmission line, and supplying said code sequence to said first or second decoding means without changing the order of said information words of said code sequence.
9. A device according to claim 7, wherein said information word is video information, and the infor-

mation amount of said first word group corresponds to said video information of one horizontal scan line.

10. A device according to claim 5, wherein said first error correction code is an inner code, and said second error correction code is an outer code.
11. A device according to claim 7, wherein said second decoding means includes a multiplier for multiplication of said information word and said parity word constituting said second error correction code by a generation matrix, and an accumulator including a delay circuit having a delay time longer than a period corresponding to $(j - 1) \times i$ words and an adder, and said second decoding means corrects an error using a syndrome outputted from said accumulator.
12. An error correction code decoding device, comprising:
 - (a) first decoding means for decoding a first error correction code which is a first parity code added to a first code group having a predetermined number of consecutive information codes of a code sequence; and
 - (b) second decoding means for decoding a second error correction code which is a second parity code added to a second code group having information codes each derived from a first group among a plurality of consecutive code groups of said code sequence.
13. An error correction code encoding device or method in which a first correction code and a second correction code are added to incoming data, characterised in that
 - if the incoming data is arranged as an array the first correction code is based on consecutive data items in a line through the array in a first direction, and the second correction code is based on non-consecutive data items in a line through the array in a second direction.
14. A device or method according to claim 13 in which the second correction code is based on every n -th data item in a line through the array in the second direction, where n is an integer.
15. An error correction code decoding device or method suitable for decoding data which has been error correction code encoded by a device or a method according to claim 13 or claim 14.
16. An error correction code encoding and/or decoding device or method in which data is correction code encoded or decoded and re-ordered, characterised in that

data is re-ordered before correction code
encoding and after correction code decoding.

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FIG. 1 PRIOR ART

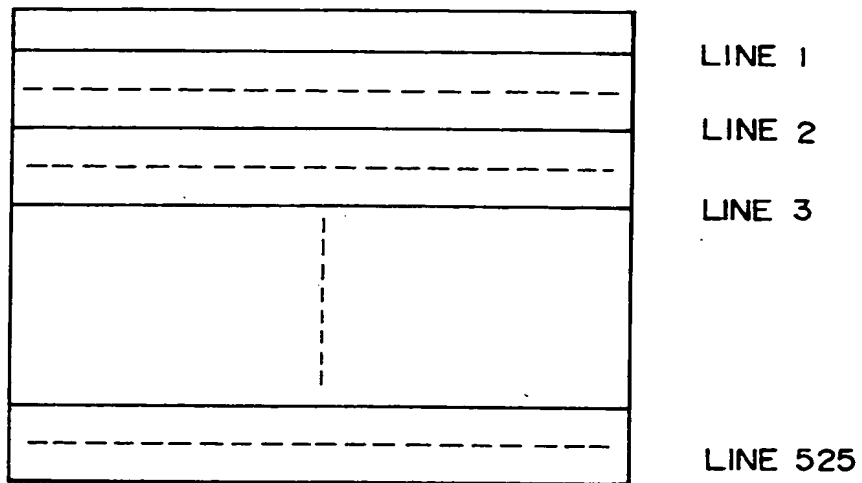


FIG. 2 PRIOR ART

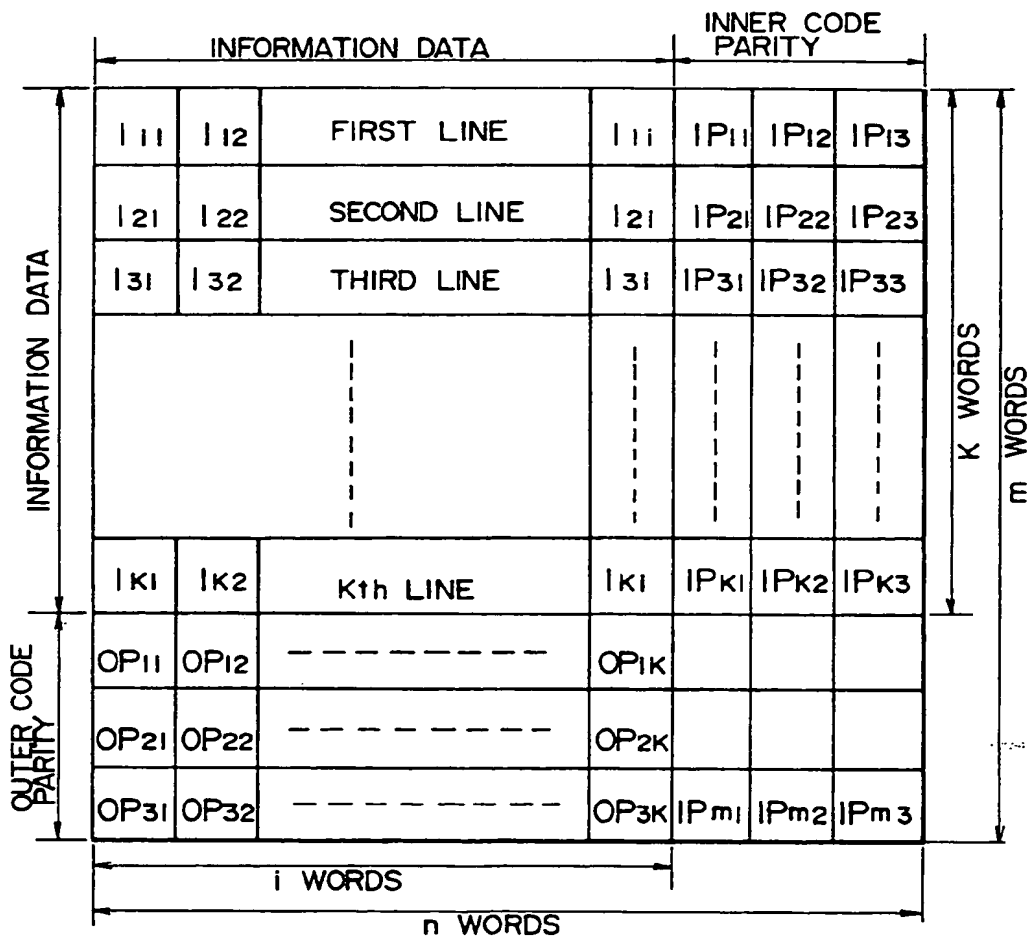


FIG. 3 PRIOR ART

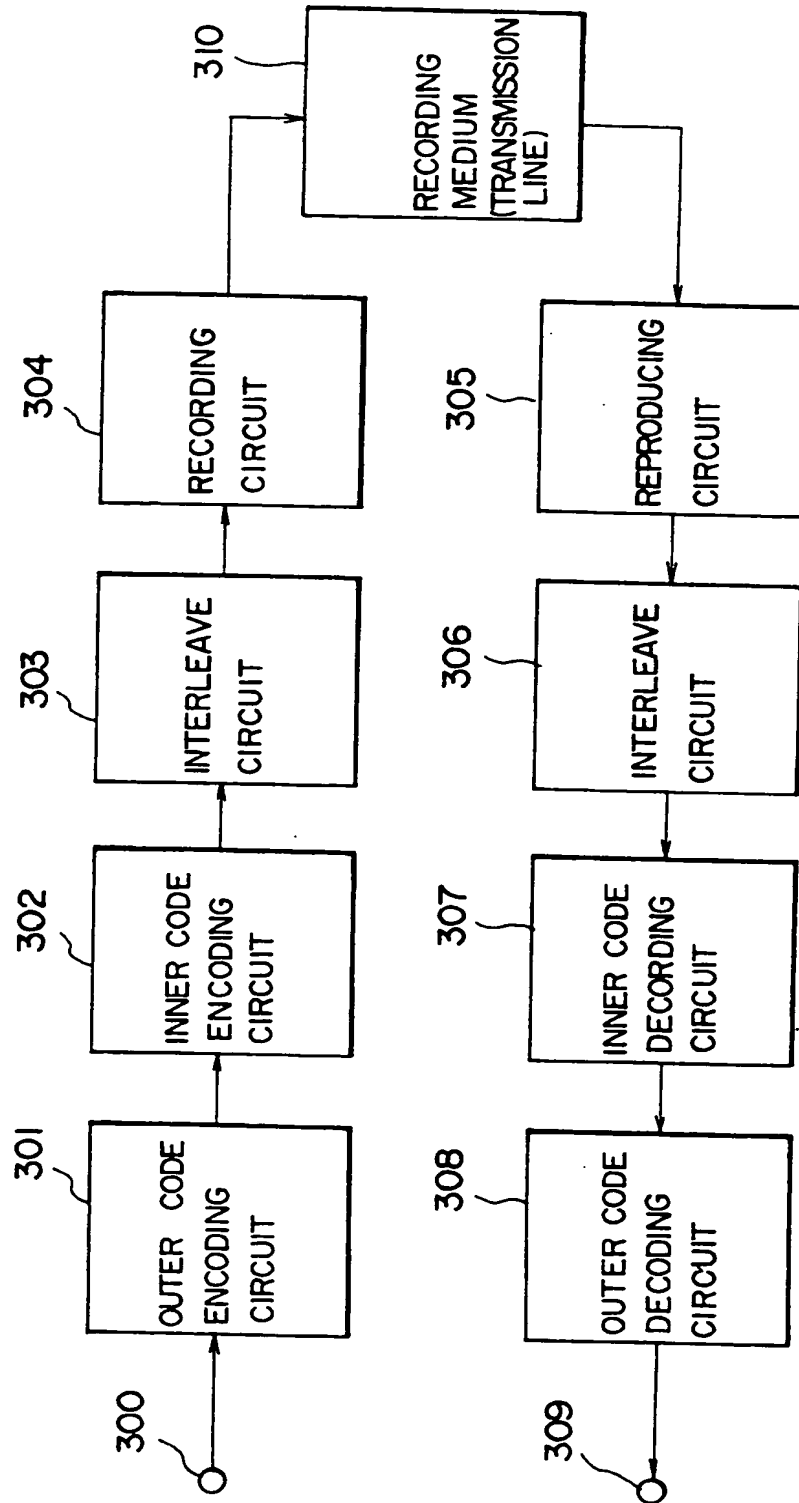


FIG. 4

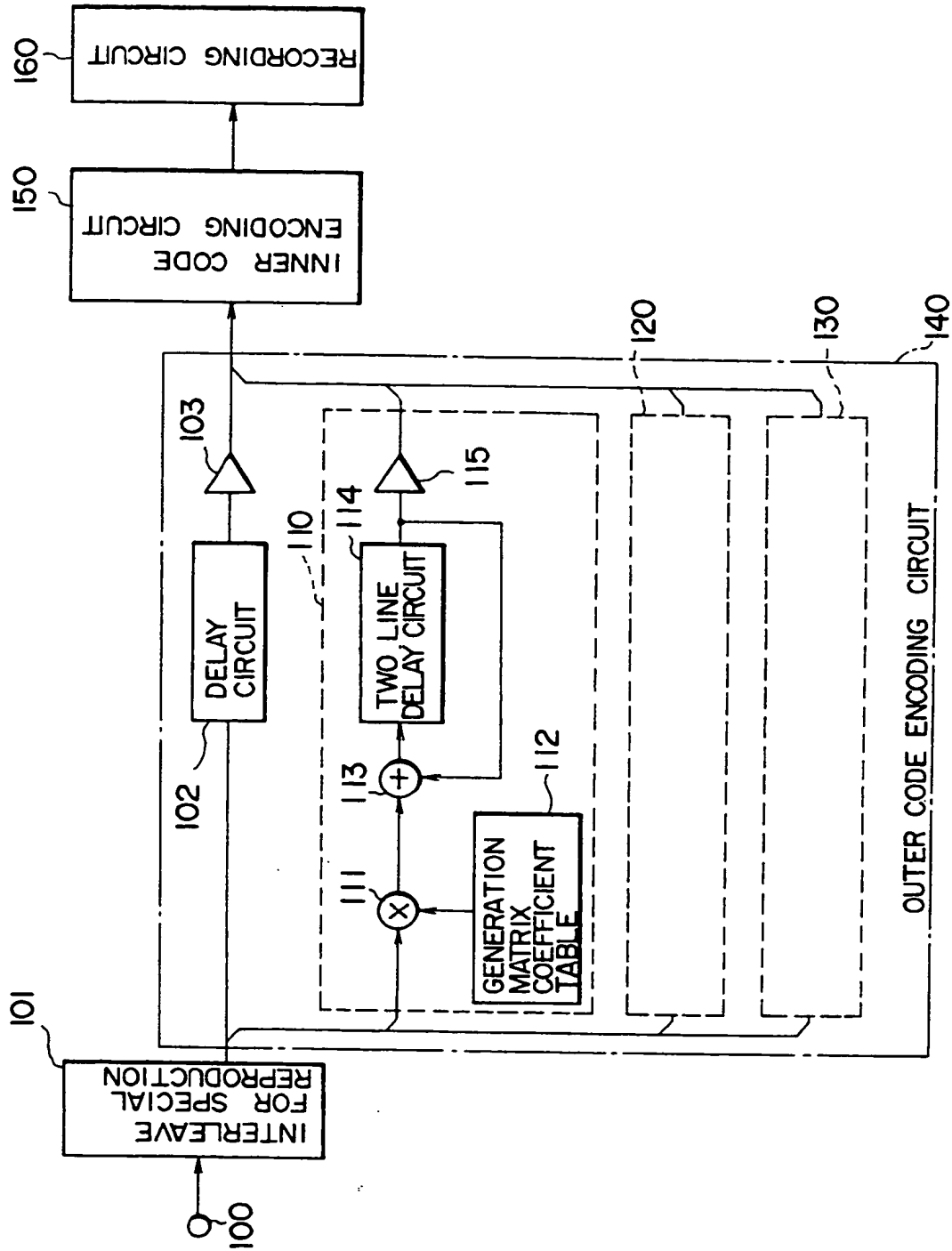


FIG. 5

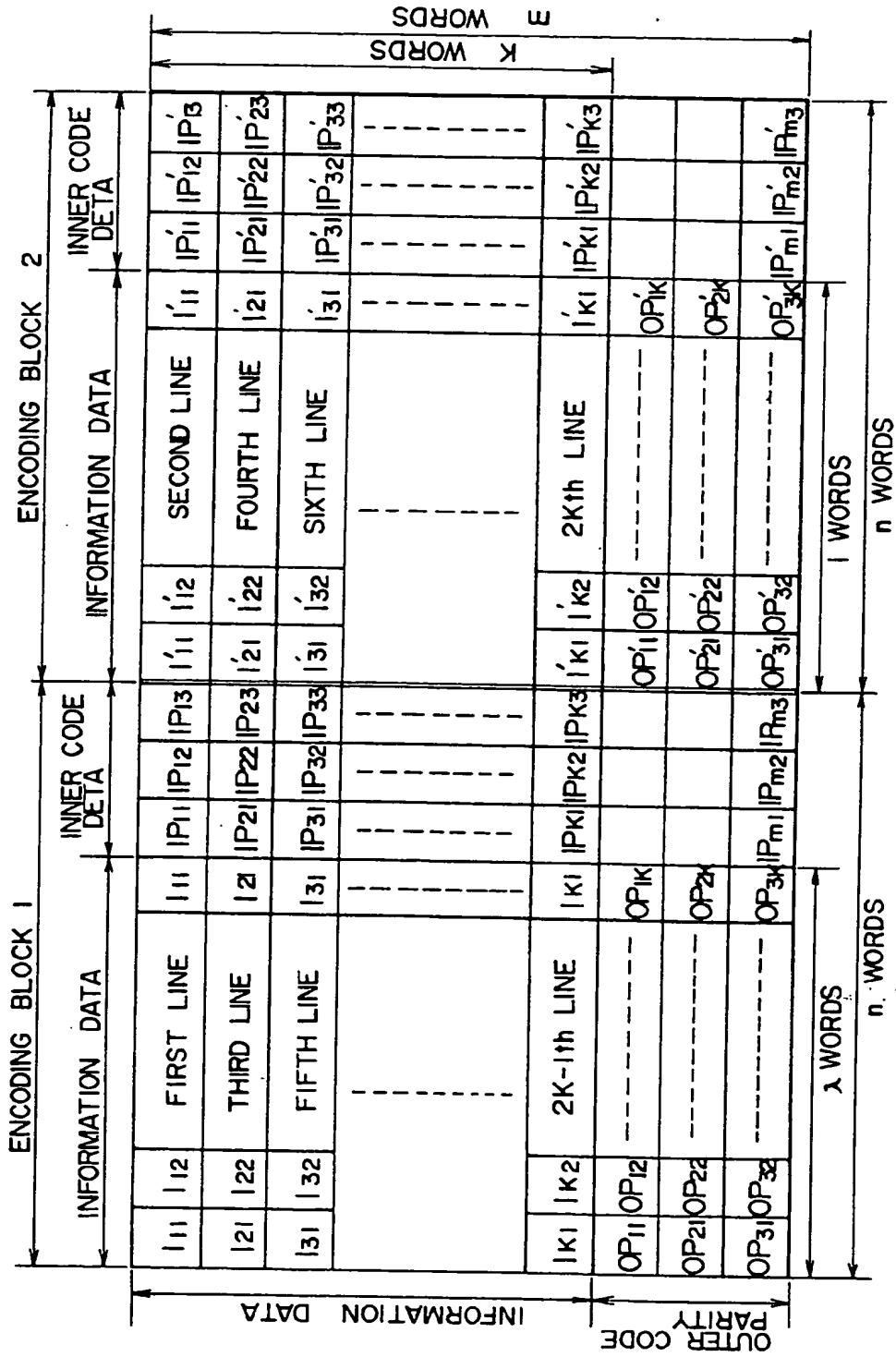


FIG. 6

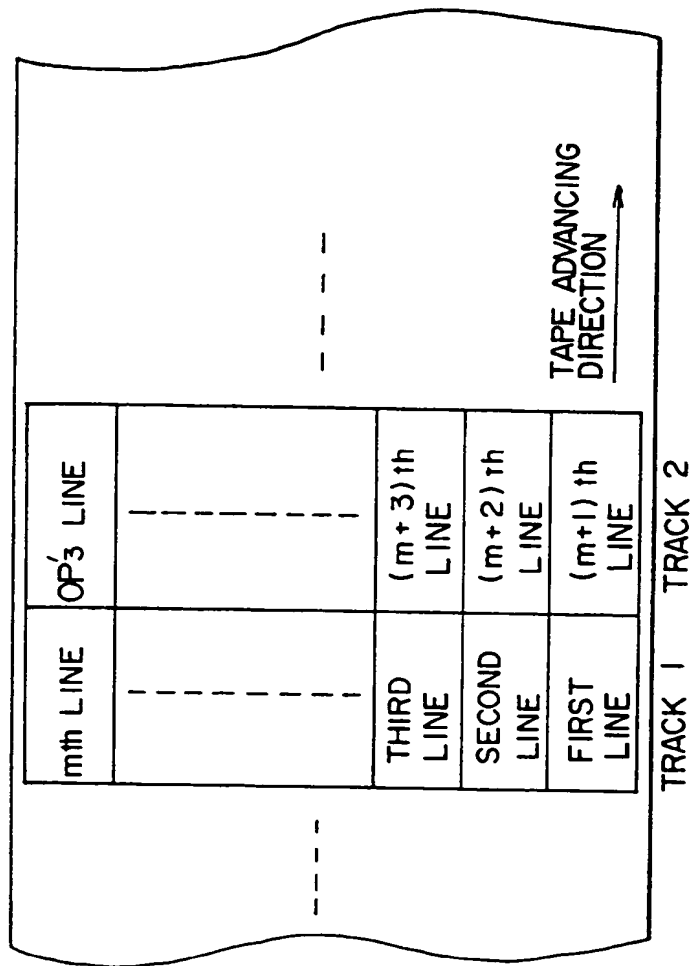
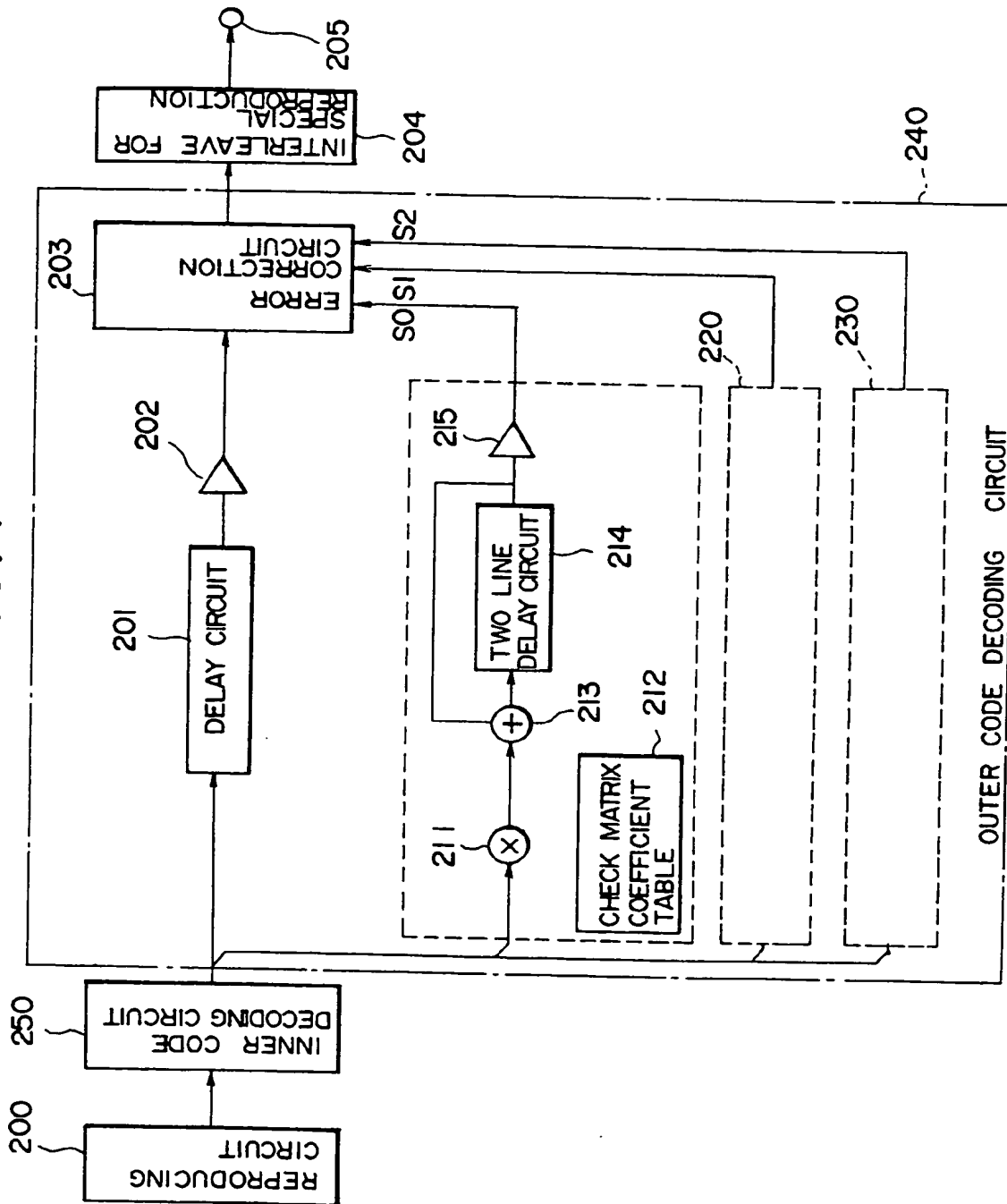


FIG. 7





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Application Number

EP 91 30 9522

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
X	EP-A-42121 (LICENTIA PATENT-VERWALTUNG) * abstract * * page 5, line 13 - page 7, line 9; figures 1, 2 *	16	H03M13/00
X	EP-A-191410 (HITACHI) * abstract; figure 4 *	1, 2, 4, 12	
X	GB-A-2065416 (SONY) * abstract; figure 13 *	5, 7, 9, 10, 3	
A	EP-A-341851 (DEC) * abstract; figures 2, 3 * * column 4, line 19 - column 4, line 50 * * column 6, line 17 - column 9, line 4 *	1, 5, 7, 10, 12, 13	
			TECHNICAL FIELDS SEARCHED (Int. Cl.5)
			H03M G11B
The present search report has been drawn up for all claims			
Place of search BERLIN		Date of completion of the search 15 JANUARY 1992	Examiner SAAM C.
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